ECONOMIC AND TECHNICAL ADVANTAGES OF REDUCTION METHOD FOR PARAMETRIC DEVIATIONS DUE TO TECHNOLOGICAL IMPERFECTION IN COMPARATOR

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Key words: Monte-Carlo analysis, lithography process deviations, comparator, hysteresis.

Introduction. The IC market is constantly growing. Today, companies whose circuits are not flexible and stable are not considered competitive. The only way to develop a more competitive product is to develop a circuit that meets stability and reliability standards. Nowadays semiconductor devices sizes in integrated circuits (IC) reached up to 2nm [Song, 2019, 1-2] and parameters characterizing the reliability and speed of the circuits, even in case of small deviations of the technological processes, may violate to an unacceptable extent from their characteristic values [Champac, 2018, 185]. Such deviations may be caused by random technological imperfections, and the main causes of this deviations are lithography and ion implantation processes random variations. So, it is very important economic condition to design circuits that are protected against technological imperfections (TI), otherwise those type of circuits [Greenstein, 2021, 130-132] will be uncompetitive against TI protected circuit in the market.

Review of literature. At the stage of development of modern IC's, the methods of lithography have reached very high accuracy, but at the same time, the sizes of semiconductor devices are reduced to a few nanometers. In this case the wavelength of light begins to exceed the dimensions of the device, and as a result of diffraction phenomenon, the contours of circuit elements and interconnections became more distorted. In order to reduce the effect of diffraction, the modern lithography process instead of light often uses shorter wavelength beams such as electron beams, X-rays. Despite the use of these approaches, it becomes almost impossible to maintain clear contours during lithography because of devices sizes. Lithography variations directly affect on the output current of transistor, since that current is proportional to the ratio W/L.

One of the important stages of the CMOS technological process is ion implantation, through which the enrichment zones or in other words doping pockets (n+ or p+)

being obtained in semiconductor devices. The main reason of ion implantation deviations is the random distribution of atoms in the doping pockets. During this process charge carriers number and threshold voltage being changed. As shown in figure 1, in the case of relatively large technological processes, the number of atoms is higher, and its deviations have a very small effect on the threshold voltage. In the case of technologies with lower dimensionality, these deviations become significant.

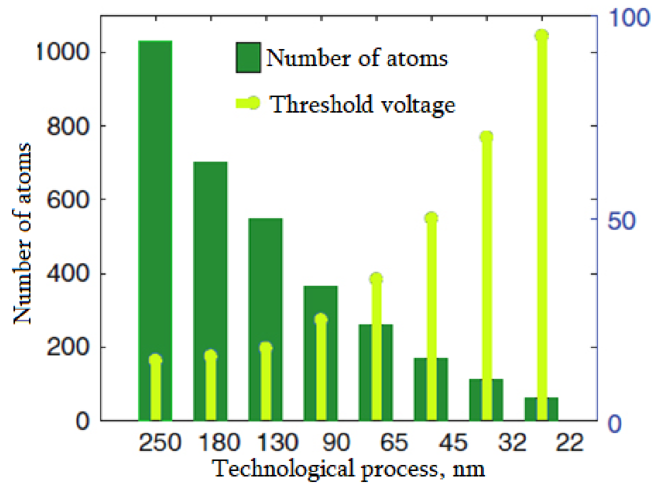

Figure 1. Dependence of threshold voltage deviation and the number of atoms on the technological process.

The modeling of the deviations described above during the production of IC is done by Monte-Carlo analysis [Turi,2017,56-59]. In Monte Carlo analysis, the entire system is simulated multiple times, where each simulation is equal to an implementation of the specified system with probability, and for each implementation all uncertain parameters are digitized.

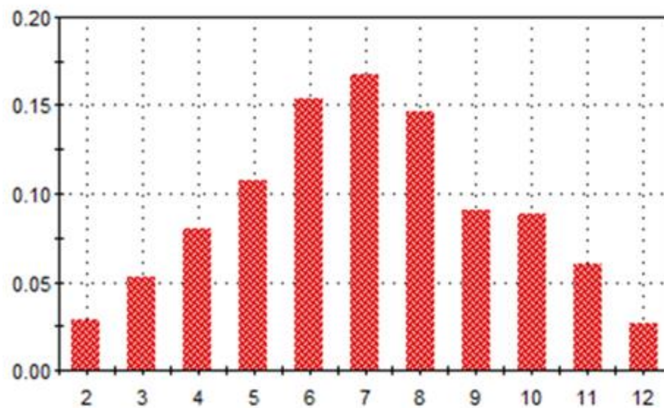

Figure 2. Probability distribution during Monte-Carlo analysis.

As a result, implementation of the independent system is collected in the probability distribution of possible outcomes (Figure 2).

Methodology. Parametric deviations due to technological imperfection were considered on the example of a comparator [Rezapour, 2018, 1-5], because one of the main disadvantages of this scheme is the dependence of its hysteresis characteristic value on deviations caused by the imperfection of the technological process. A comparator is designed to compare the analog signals given on its two inputs and obtain a digital signal at the output. If the potential applied to the positive input of the comparator is greater than the potential applied to the negative input, then a logic "1" signal will be obtained at the output of the circuit, otherwise, a logic "0" signal. Comparator circuit is considered economically advantageous, as it has a low cost and high demand. Comparators as shown in figure 3, generally consist of three main parts. In first stage is located preamplifier which is used to amplify the input signal, as a result comparator sensitivity increasing. Also, the preamplifier isolates the comparator from kickback noises. In second part located latch, which is the main circuit performing the comparison function. Latch should distinguish even the smallest difference between the voltages of the input signals. In the last cascade of high-speed comparator is located output buffer. The main function of the output buffer is to convert the signal received from the output of the latch into a digital signal.

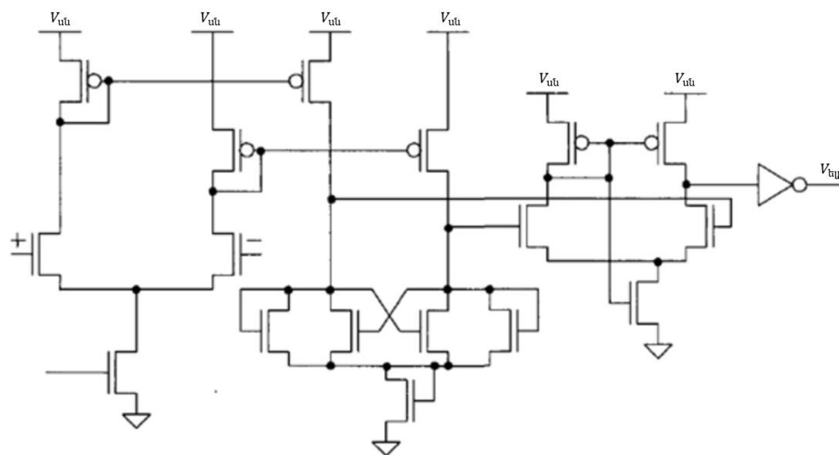

Figure 3. Comparator circuit.

Comparators are often placed in a noisy environment (input signals contain noise) and if the circuit is high-speed and the noise in turn contains large amplitudes, the output will also be noisy. Hysteresis effect is often used to avoid noise at the output. Hysteresis is a comparator property whereby the switching voltage is a function of input or output voltage levels. The main drawback of circuit presented above is the strong dependence

of the hysteresis width on the deviations caused by the imperfection of the technological process.

Scientific novelty. The proposed architecture makes it possible to minimize the effect of deviations caused by the imperfection of the technological process without significant surface changes on the semiconductor crystal. The improvement proposed in the article should improve the implementation of comparator and make this product more competitive and reliable in the market.

Analysis. The main principle of the proposed method is that the hysteresis is obtained by changing the reference voltage depending on the signal edge.

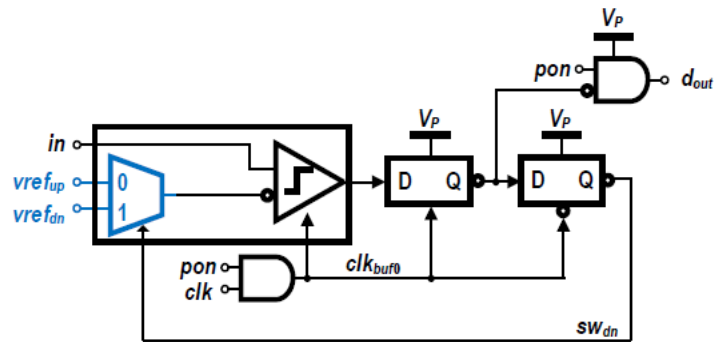

Figure 4. Proposed circuit.

In this scheme, the main comparison operation is performed by high-speed clocked comparator, which improves the overall system input/output delay compared to other schemes. The signal applied to the input of this circuit first of all being compared with $vref_{up}$ voltage level, then the comparison signal is being transferred to the digital circuit, which consists of two anti-phase clocked D-triggers. The first D-trigger reads the clock signal at a positive level and transmits the data received from the switch to the output, and the second trigger switches based on the received data switching sw_{dn} signal by changing reference voltage from $vref_{up}$ to $vref_{dn}$. As a result, the hysteresis value will be equal to`

$$V_{hyst} = vref_{up} - vref_{dn}$$

Circuits were designed with Synopsys Custom Designer [Synopsys, 2014, 236] tool and simulations have been verified by Synopsys Hspice [Synopsys, 2017, 846] circuit level simulator. During the simulation,3 possible cases were considered for the scheme verifications (table 1).

Table 1. Processes considered during comparator verifications.

Process	NMOS/PMOS	Reference voltage	Temperature
Typical	Typical/Typical	0.8mV	25 °C
Slow	Slow/Slow	0.66mV	-40°C
Fast	Fast/Fast	0.93mV	125°C

During simulations, input hysteresis was considered as the main parameter, the results of which are described in table 2 for reference circuit and in table 3 for proposed circuit.

Table 2. Input hysteresis value for reference comparator

Parameter/Process	Typical	Slow	Fast
Hysteresis(mV)	71.38	64.05	54.44
Hysteresis deviation (mV)	4.8	5.1	3.5

Table 3. Input hysteresis value for proposed comparator

Parameter/Process	Typical	Slow	Fast
Hysteresis (mV)	50.27	47.78	47.87
Hysteresis deviation (mV)	3.02	2.9	3.04

As shown in table 2 and in table 3 the proposed comparator circuit became more flexible in harsh environments, there is improvement from 31.2mV variation between typical/slow/fast cases to 5.51mV. Thus, making the product more competitive not only for standard condition environments, but also for non-standard environments where can be observed extreme temperature and voltage values. The changes proposed in the article improve the implementation of comparator and make this product more competitive. However, in contrast to the improvements, there are also drawbacks. Improvements have been made by increasing the surface area of the circuit.

The information about the deviations caused by the imperfection of the technological process in the reference and proposed comparators is represented by the distribution diagrams of the Monte-Carlo method in figure 5 for the reference circuit and in

figure 6 for the proposed comparator. Distribution diagrams shows that proposed comparator circuit is more reliable against technological imperfection caused by lithography and ion implantation processes random variations.

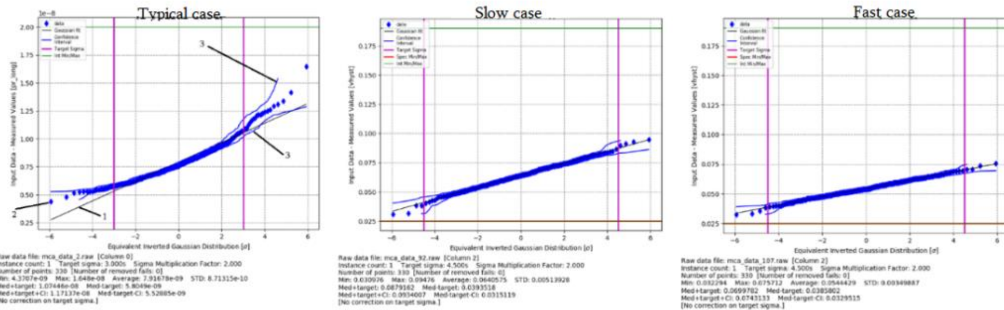

Figure 5. Input hysteresis distribution diagram for the reference comparator, typical/slow/fast cases

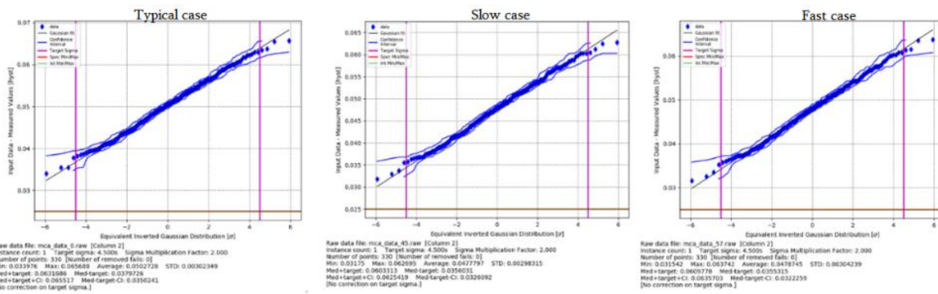

Figure 6. Input hysteresis distribution diagram for the proposed comparator, typical/slow/fast cases

Conclusion. The proposed comparator scheme makes possible to minimize the effect of deviations caused by the imperfection of the technological process without significant surface changes on the semiconductor crystal. Usage of recommended comparator makes possible to reduce the hysteresis deviations from 31.11% to 5.21%. The proposed comparator scheme requires an additional 19% space over the existing scheme. Thus, using the proposed approach, it is possible to significantly reduce the market value of an integrated circuit by increasing the demand and competitivity for circuits with protections against technological imperfection .

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Economic and Technical Advantages of Reduction Method For Parametric Deviations Due to Technological Imperfection in Comparator

Key words: Monte-Carlo analysis, lithography process deviations, comparator, hysteresis

Nowadays devices sizes in integrated circuits (IC) have reached up to 2nm [1]. In this case, the parameters characterizing the reliability and speed of the circuits, even in the case of small deviations of the technological processes, may violate to an unacceptable extent their characteristic values [2]. Such deviations may be caused by random technological imperfections. The modeling of the deviations described above is done by Monte-Carlo analysis [3]. Parametric deviations due to technological imperfections were considered and minimized on the example of the comparator [4], because one of the main disadvantages of this scheme is the dependence of its characteristic values on deviations caused by the technological process imperfections. The proposed comparator scheme makes it possible to minimize the effect of deviations caused by the imperfection of the technological process without significant surface changes on the semiconductor crystal. By using the scheme of the proposed comparator, it was possible to reduce the hysteresis deviations from 31.11% to 5.21%. The proposed comparator scheme requires an additional 19% space against the existing scheme.