ECONOMIC EFFICIENCY OF VOLTAGE AND TEMPERATURE DRIFT COMPENSATION CIRCUIT FOR DIGITAL DELAY LINE

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Key words: Ser-Des, voltage variations, temperature variations, digital delay line, compensation circuit, clock delay, data delay

Introduction. The Integrated Circuits (IC) market is one of the crucial parts of Information Technology (IT) industry. Nowadays With market demand, the IC development industry has been experiencing rapid growth and improved general competency. The IC market and manufacturing industry have been keeping pace with global development and often integrated circuits are being used in non-standard environments. The development of the proposed voltage and temperature drift compensation circuit (VTDCC) has become an economically important condition [Steinmueller,1992, 327–349], because VTDCC allows the digital delay line (DDL) to work correctly in non-standard conditions, which increases the demand for DDL. One of the biggest disadvantages of architecture without VTDCC above is instability in case of nonstandard conditions. It means there can be temperature and voltage drifts, which in turn will effect on delay of the cell so it is necessity to have voltage-temperature (VT) compensation circuit, otherwise DDL will lose its effectiveness.

***Review of literature*.** Nowadays when transistor sizes reached up to 2nm [Song, 2019, 1-2] high speed Ser-Des systems became less power-consuming, began to work with lower supply voltages and systems operating frequencies reached dozens of gigahertz [Patel,2010,2-4]. Despite these advantages, it became more complicated to meet stability, reliability, and timing constraints in the system. High operating frequencies lead to clock and data signal misalignment because of clock skew phenomenon. It means clock signals have phase shift in different points of clock path. One of the commonly used circuits to overcome this problem is DDL[Pasha,2015,1-4] circuit (figure. 1) .

Methodology. This circuit is considered economically advantageous, as it has a low cost and high demand. DDL circuit design contains serial connected even number

voltage-controlled delay cells, which allow DDL to correctly shift clock signal and sample it with data.

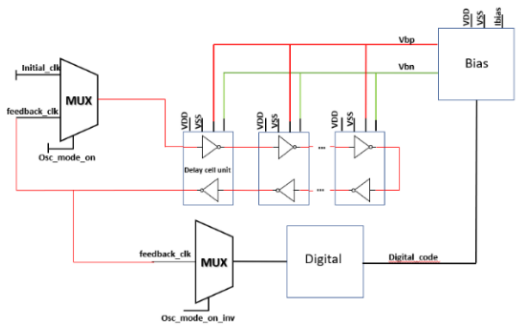

Figure 1. Digital delay line

At the initial stages DDL acts as oscillator and starts calibration process by comparing reference clock with feedbacked output clock. Often integrated circuits (IC) being used in non-standard environments. It means after calibration there can be temperature and voltage drifts, which in turn will affect the delay of cell. DDL provided delay values in standard conditions presented in Table 1.

Process	Voltage (mV)	Temperature (°C)	DDL provided delay (ps)
TT	0.75	25	1405
SS	0.625	-40	1321
FF	0.845	125	1463

Table 1. DDL operation during standard conditions

To understand how circuit will function in case of non-standard conditions, simulations have been verified for DDL in VT drift conditions. Maximum violation of delay provided by DDL, observed during 0.625mV to 0.75mV voltage drift where delay value changes from 967ps to 1893ps.

Scientific novelty. Currently the IC market is constantly growing and companies whose semiconductor devices are not flexible in case of non-standard conditions are not considered competitive. The only way to develop a more competitive product is to develop a circuit that meets stability and reliability standards in harsh environments. The proposed architecture makes it possible to minimize the non-standard conditions effect on DDL circuit. The method proposed in the article should improve the implementation of DDL and make this product more competitive and reliable in the market.

Analysis. To reduce VT drift effect on DDL circuit operating process, compensation circuit is proposed in this paper. Main principle of proposed circuit (figure

2) is to sense delay variation by comparing initial clock against single delay cell output. According to this difference, the delay cell's reference voltage will be increased or decreased.

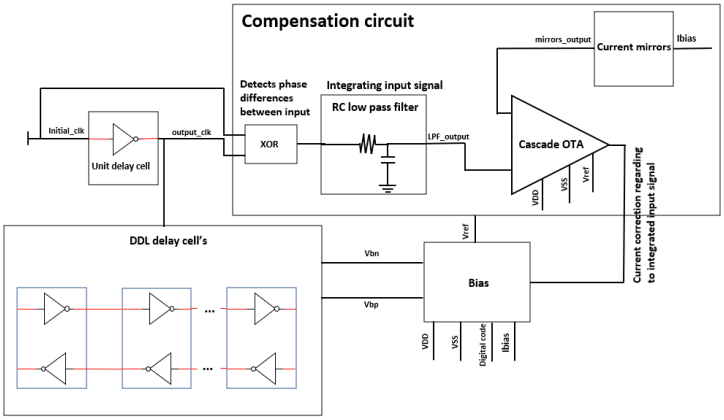

Figure 2. DDL proposed circuit with compensation.

To sense delay variations, in the first stage of compensation circuit phase detector (PD) is used. There are two variants for digital PD circuits. XOR circuit can be used as PD by sensing input signal differences in case of low bitrates. Main advantage of this circuit is uncomplicated design, which leads to less power consumption, and low market value.

Unfortunately, XOR circuit consists of drawbacks, which makes XOR usage in case of high bitrates not effective. First of all, one of the widespread issues that can be faced in XOR logic gate that acts as PD is large dead zone range. It happens because XOR cannot detect small differences in phases between two input clocks, and as a result glitches being created by logic gate on his output (figure 3.) [8]. If the phase detector is operating in the dead zone region, it cannot detect phase errors and the compensation circuit will be locked to the incorrect phase. The second drawback of this type of phase detector is sensitivity to the input clock duty cycle, which means duty cycle should be around ~50%. That's why more reliable and sensitive PD should be designed to detect any phase differences in case of high bitrates.

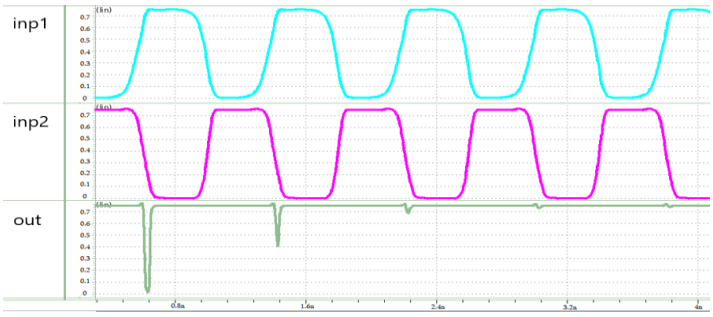

Figure 3. Dead zone observed in XOR during simulations.

To overcome the issue described in high-speed systems phase-frequency sensitive detectors can be used as PFD (figure 4). Mostly these circuits have insignificant small dead zone range. Phase-frequency detectors are widely used in DDL/PLL systems because of their high performance.

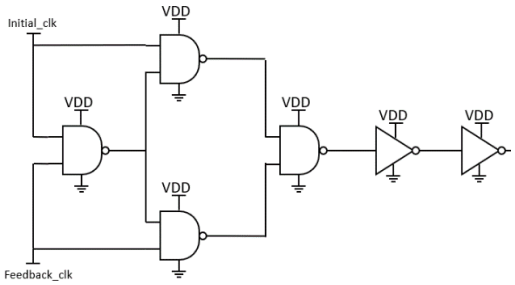

Figure 4. PFD architecture

PFD output is given to integrator circuit which controls operational transconductance amplifier (OTA) (figure 5) input, which helps to compensate delay changes by controlling current mirror logic during temperature and voltage drifts.

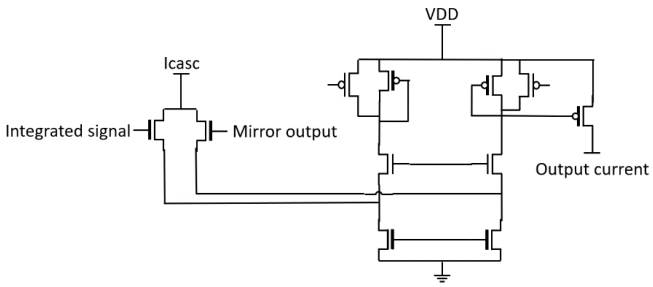

Figure 5. OTA schematic

This section presents simulation results for proposed compensation circuit. 7nm technology node circuit was designed with Synopsys Custom Designer tool [Synopsys,

2014, 236] and simulations have been verified by Synopsys Hspice circuit level simulator [Synopsys, 2017, 846]. Verifications are done for 18 PVT (Process, Voltage and Temperature) cases, including NMOS/PMOS – typical/typical, slow/slow, fast/fast corners, 3 standard temperature environments - high (±125°C), typical (±25°C), low (±40°C), 3 supply variations for reference voltage - Min (VDD = 0.666mV), typical (VDD = 0.8mV),Max(VDD=0.93mV) and during simulation temperature and voltage was been swept to imitate VT drift. 'Table 2' shows simulation results that measures delay during temperature and voltage drift.

Drift	Proposed circuit min. variation delay (ps)	Proposed circuit max. variation delay (ps)
0.625mV to 0.75mV	1426	1496
0.75mV to 0.875mV	1437	1462
± 25 °C	1432	1491
± 40 °C	1435	1453
± 125 °C	1441	1491

Table 2. DDL compensation circuit during temperature/voltage drift

As shown in table 2 proposed circuit became more flexible and reliable in harsh environments. Thus, making the DDL circuit more competitive not only for standard condition environments, but also for non-standard environments where extreme temperature and voltage drifts can be observed. The method proposed in the article improves DDL operation and makes this product more competitive. However, in contrast to the improvements, there are also drawbacks. Improvements have been made by increasing the DDL area. One of the main parameters in VT compensation circuit are OTA AC parameters. OTA gain, and other AC parameters during operation in feedback system presented in 'Table 3'.

AC parameter	Values for Cascade OTA
Gain	55 dB
Phase margin	59 deg
Gain margin	12.1 dB
PSRR	≤ -26dB

Table 3. Cascade OTA AC parameters

Conclusion. The proposed compensation circuit makes correct DDL operation possible in case of non-standard conditions. Main principle of this circuit is to sense delay variation by comparing initial clock against single delay cell output. According to this difference, the delay cell's reference voltage will be increased or decreased. DDL with included compensation circuit has shown around 51% DDL delay range improvement during VT non-standard conditions (maximum variation observed during 0.625mV to 0.75mV voltage drift where delay value changes from 967ps to 1893ps.). Compensation circuit requires an additional 37% area in DDL circuit. Thus, using the proposed approach, it is possible to significantly reduce the market value of an integrated circuit by increasing the demand for DDL.

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Nowadays when semiconductor devices sizes reached to the few nanometers, high-speed SERDES systems became less power-consuming, and systems operating frequencies reached dozens of gigahertz. Despite these advantages, devices became more vulnerable against temperature-voltage drifts. Also, because of dozens of gigahertz frequency data transmission, it became more complicated to meet timing constraints in Serdes systems. Therefore, it is important to have stable de-skew mechanisms, otherwise data loss and other timing issues can be observed. One of the commonly used circuits to overcome this problem is digital delay lines (DDL). Often integrated circuits (IC) being used in non-standard environments, so it is necessity to have voltage-temperature (VT) compensation circuit (VTDCC), otherwise DDL will lose its effectiveness. The development of the proposed of VTDCC has become an economically important condition, because VTDCC allows digital delay line (DDL) to work correctly in non-standard conditions, which increases the demand for DDL. Digital delay line with included compensation circuit has shown around 51% DDL delay range improvement during non-standard conditions VT drift compensation circuit requires an additional 37% area in DDL.