ECONOMIC SIGNIFIANCE AND DESIGN OF LOW AREA AND LOW POWER MAGNITUDE COMPARATOR

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Key words: Digital comparator, logic gate, transistor logic, SAED 32/28 nm

Introduction. The digital comparator is one of the most widely used combination circuits in electronics, designed to compare two binary numbers [Rajesh, 2014, 238-247, Parashar, 2015, 977 – 982]. A typical digital comparator contains NOT, AND, XOR, NOR logic gates that compare the digital signals present at their input terminals and produce an output depending upon the condition of those inputs.

For example, along with being able to add and subtract binary numbers we need to be able to compare them and determine whether the value of input A is greater than, smaller than or equal to the value at input B etc. The digital comparator accomplishes this using several logic gates that operate on the principles of Boolean Algebra. Comparators are used almost everywhere, especially they are irreplaceable in ALUs (Arithmetic Logic Unit), that is used in different architectures of processors, microprocessors, and microcontrollers.

***Scientific novelty*.** Currently the electro energy is turning into one of the most important parts of the economy. That is why our study is aimed to design electrical schemes and components that attempt to further minimize the power consumption in their designs, given the fact that the number of transistors is continuously increasing in integrated circuits. To achieve power minimization, we are constantly improving low power designs, which helps to decrease the power consumption in electrical systems.

Table 1. Truth table of identical comparator

Input		Output
A	B	A
0	0	0
0	1	0
1	0	1
1	1	1

Types of comparators. There are two types of digital comparators: identical comparator and magnitude comparator. Both types make comparisons, but they are somewhat different. After comparing the numbers, the identical comparator generates 1 signal at the output, which indicates whether the input binary numbers are equal or not. Table 1 shows the truth table of 1-bit identical comparator.The magnitude comparator, unlike the identical comparator, generates 3 signals at the output during the number comparison, showing that the first number is greater than the second, less or equal. The truth table of 1-bit magnitude comparator is presented in Table 2.

Table 2. Truth table of magnitude comparator

Input		Output		
A	B	A	B	A
0	0	0	0	0
0	1	0	1	0
1	0	1	0	1
1	1	1	1	1

Figure 1 shows a 4-bit magnitude comparator gate level logic circuit. The circuit consists of 8 NOT, 4 2-input XOR, 2 2-input AND, 2 3-input AND, 3 4-input AND, 2 5-input AND, 2 4-input OR logic gates.

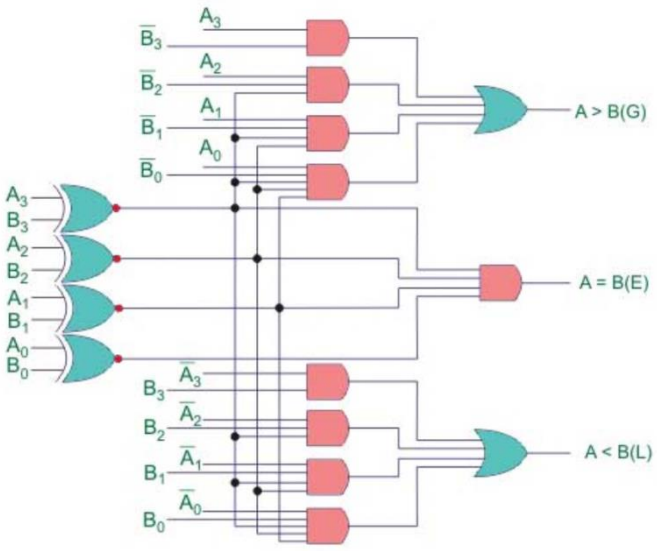

Figure 1. Gate level circuit of 4-bit magnitude comparator

If we calculate the total number of transistors, that is needed to make this circuit, then we will get: 8 * 2 + 4 * 8 + 2 * 6 + 2 * 8 + 3 * 10 + 2 * 12 + 2 * 10 = 150 transistors, which is a quite big number, taking into account the fact that technologies nowadays become smaller and smaller and the problem of circuit area becomes more significant.

Proposed architecture. There are special transistor logics that allow us to reduce the number of transistors in a single logic gate. Figure 2 shows NOR and AND logic gates that are designed using PTL (Pass Transistor Logic) and DVL (Dual Value Logic) logics [Bui, Wang, Jiang, 2002, 25-30, Sharma, Mehra, 2014, 57-60].

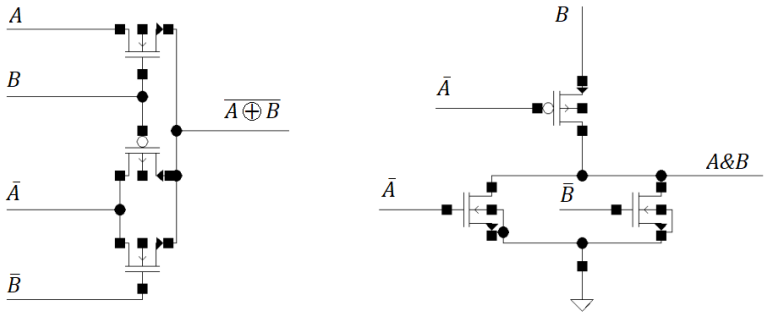

Figure 2. XOR and AND logic gates designed using PTL and DVL logics respectively

The research was conducted using Synopsys software tools. The goal of the work is to design a 3-bit comparator using a smaller number of transistors. To achieve this, some logic gates of the comparator will be represented by the mentioned PTL and DVL logics. Figure 3 shows the transistor level magnitude comparator scheme using CMOS technology. Figure 4 shows the same transistor level comparator circuit using PTL and DVL logic. The schemes were assembled using Custom Compiler software tool, and the simulations were performed with Hspice tool [Synopsys, 2018, 878].

According to the circuits, using PTL and DVL logics, the number of transistors decreases from 108 to 81. However, with PTL and DVL logics, the logic gates have a little disadvantage. Their output signals may deviate to some extent from the expected values. However, these deviations are not large enough to affect the overall functionality of the circuit. These signals pass through other logic gates, and, after making some improvements, they will finally disappear.

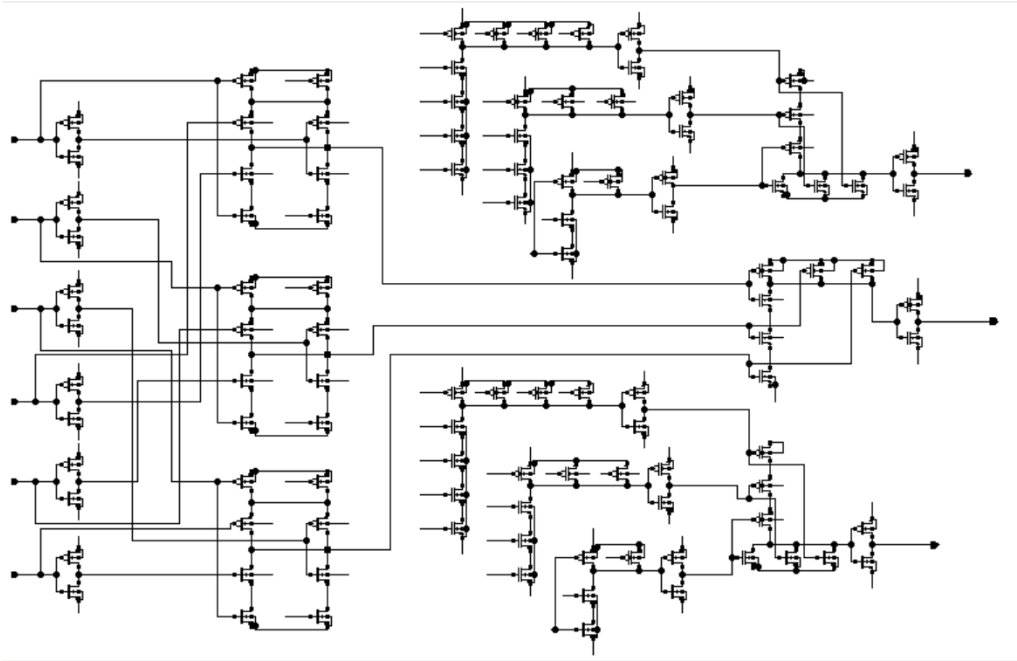

Figure 3. Transistor-level comparator circuit using CMOS technology

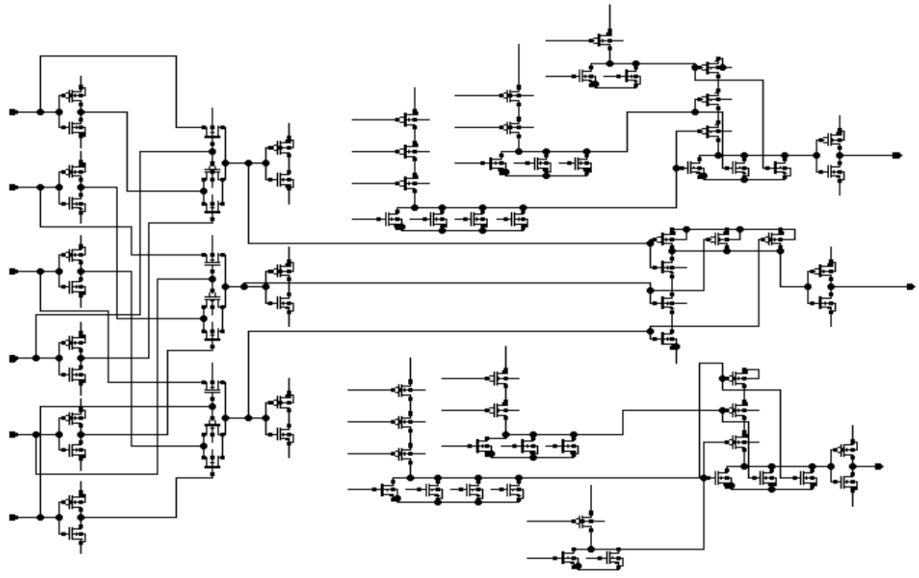

Figure 4. Transistor-level comparator circuit using PTL and DVL logics

Analysis and simulation results. Figure 5 demonstrates the input and output signals of the circuit, which is designed with CMOS technology. Figure 6 shows the input

and output signals of proposed comparator circuit. The signals were generated using Wave View software tool.

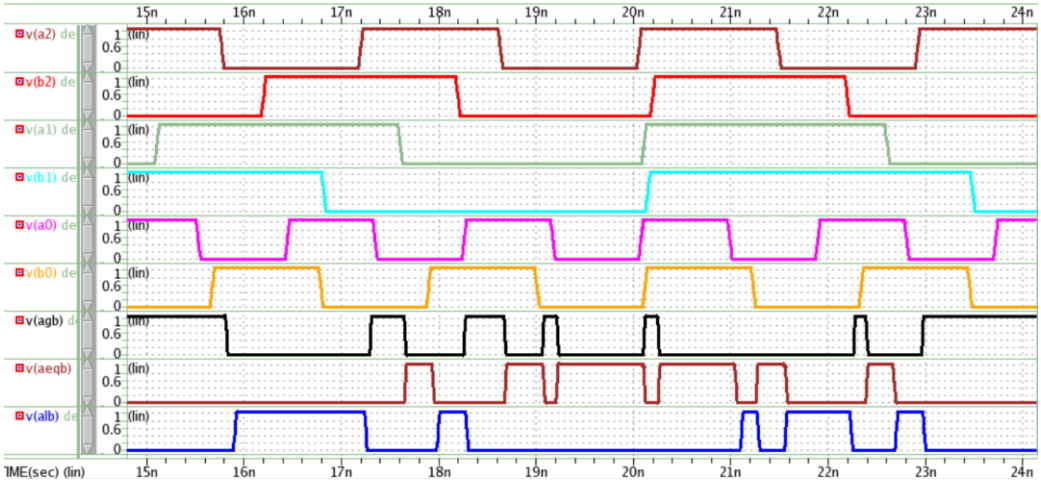

Figure 5. Simulation results of CMOS comparator

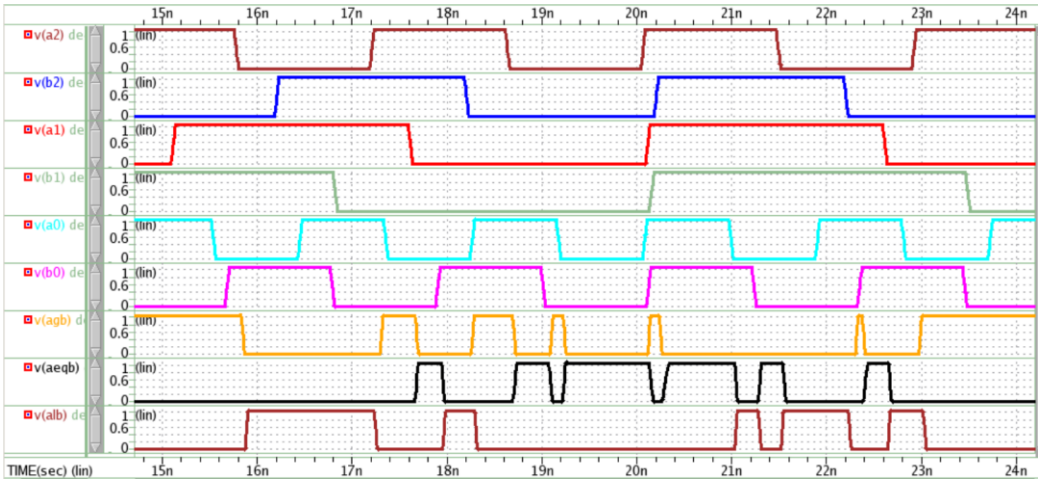

Figure 6. Simulation results of comparator circuit using PTL and DVL logics

Simulation results show that the functionality of both circuits are completely identical. Table 3 presents a comparison of some of the parameters of these 2 circuits using different logics.

Table 3. Comparison of parameters

Logic	Output load (fF)	Transistor number	Delay (ps)	Power (uWatt)
CMOS	1	108	67.9	4.5763
PTL, DVL	1	81	48.6	3.6015

Conclusion. In this article a 3-bit magnitude comparator circuit was developed, using standard CMOS technology and a new method, thanks to which, it consists of a smaller number of transistors. As a result, the circuit will occupy less area and have less power consumption. Some of the logic gates were designed using PTL and DVL logics instead of classic CMOS technology, due to which the number of transistors has been reduced from 108 to 81, or by 25%. The overall circuit delay has been decreased by 28.42% and the power was reduced by 21.3%. The circuit has been developed and simulated using SAED 32/28nm technology process.

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Design of low area and low power magnitude comparator

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Multibit digital comparators take up large surface and high power consumption. As they are composed of logic gates, it is recommended to decrease the number of transistors in the logic gates using different transistor logics. By decreasing the number of transistors, the occupied surface and power consumption of the entire circuit will also decrease. The identical circuit was propounded applying standard CMOS (Complementary Metal-Oxide-Semiconductor) technology and with a combination of PTL (Pass Transistor Logic) and DVL (Dual Value Logic) transistor logics. Due to less area and decreased number of transistors, the physical design (layout) of the whole circuit will become easier and less time consuming from layout designer point of view, then in case of standard CMOS technology. As an output load was used a 1fF capacitance for both circuits. Correspondingly, the propounded circuit cuts down the power consumption by 21.3%, the delay was decreased by 28.4%, and the number of transistors was reduced by 25%. The circuit was developed using Custom Compiler tool. All the simulations are done using Synopsys Hspice and WaveView tools. SAED (Synopsys Armenia Educational Department) 32/28 nm technology process libraries have been used during the work.