PROBLEMS OF ECONOMIC AND TECHNICAL AND EFFICIENCY OF INTEGRATED CIRCUIT PARAMETERS

Davit Babayan
Ph.D in technical science
Artur Ghazaryan
Gurgen Grigoryan
Tigran Grigoryan
NPUA, MS students

Key words: digital blocks, analog blocks, leakage power, corner, area, measurement system

Introduction. In modern economic conditions, any activity relates to economic issues. Currently, there are more and more research organizations in the field of integrated circuit design, which occupy a special place in the development of the field. At present, about 60% of IC customers list power consumption as the main problem, and area as the secondary problem. The software used to measure these parameters is a component of some expensive programs. The system presented in the paper will take its unique place in the market of low-cost devices due to its ease of use.

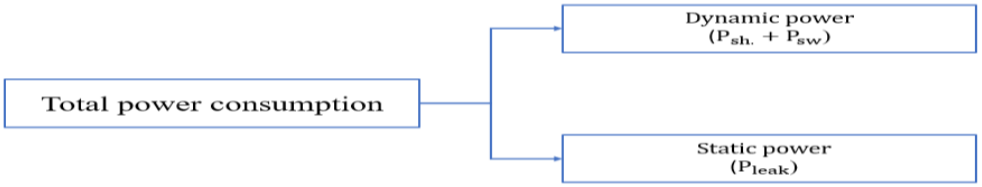

Figure 1. The total power consumption of integrated circuit

Methodology and literature review. Dynamic energy consumption is formed by the power conditioned by short-circuit and switching currents. Power due to switching current occurs when a logical level between logical 1 and logical 0 in the circuit. Short-circuit current occurs when there is a direct connection between the power supply and ground: In CMOS integrated circuits, the dynamic energy consumption mainly depends on the switching component. Power consumption due to static current of CMOS integrated circuits occurs when the circuit is connected to the power supply, but there is no switching at a logical level. The total component of the leakage current is mainly formed based on three components: the current passing through the valve, undercurrent, and the current due to the opposite deflection. The effect of the components on the output current has changed over time, in particular in the technological process above 180 nm only the undercurrent is taken into account, in the technological process above 90 nm the total scatter current is formed by the undercurrent loss current and valve loss current and below 90 nm In the technological process, the total scatter current is formed by the subthreshold current, the valve loss current, and the reverse deflection current. This is shown in Figure 2 [Agarwal et al., 2006, 692-696; Vashishtha et al., 2015; 2900-2903].

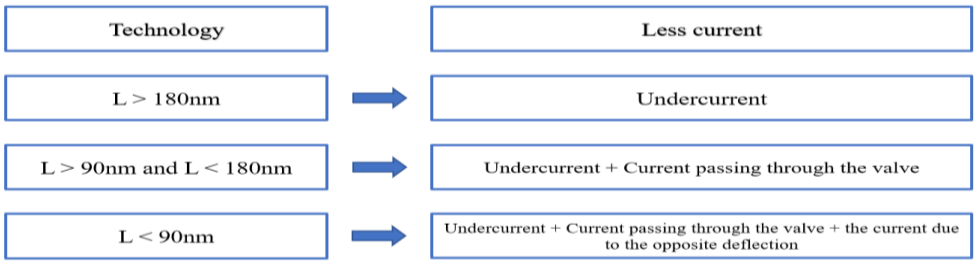

Figure 2. Leakage current

Depending on the technology, the ratio of dynamic to static energy consumption is changing, and currently static energy consumption is several orders of magnitude higher than dynamic energy consumption. Figure 3 shows the energy consumption ratio in the integrated circuit [Dilip, Prasad, Bhavani, 2012, 72-73].

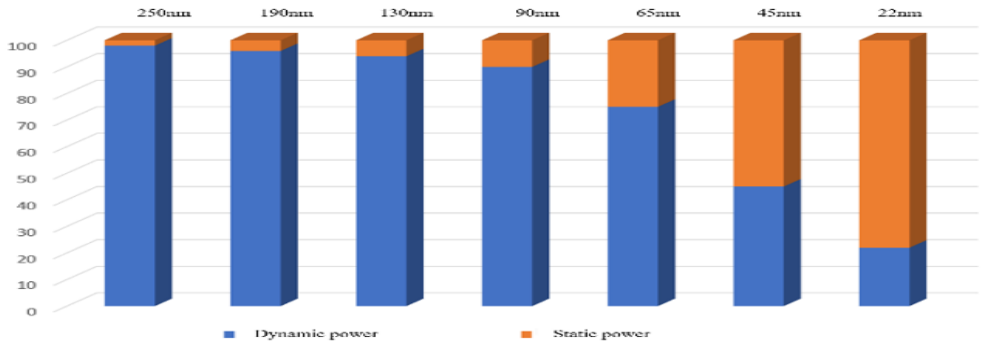

Figure 3. The Dynamic and static power consumption

The operation of measuring systems (or devices) is based on two basic principles: either system speed or system accuracy. For large designs, accurate measurements take quite a long time (for it me use spice simulations), and the designer needs measurement results at different stages of the design process. Therefore, it is necessary to have a system that will perform fast measurements, the amount of allowable error. At present, integrated circuits have both digital and analog nodes. The design of digital circuits is mainly done using electronic automated design software, for which the input information is the behavioral presentation of the circuits in Verilog, VHDL languages, the constraint file, as well as the libraries of standard elements that we will use during the measurements [Chukhajyan, 2014;13-21].

Proposed algorithm. This is the proposed algorithm of the presented system:

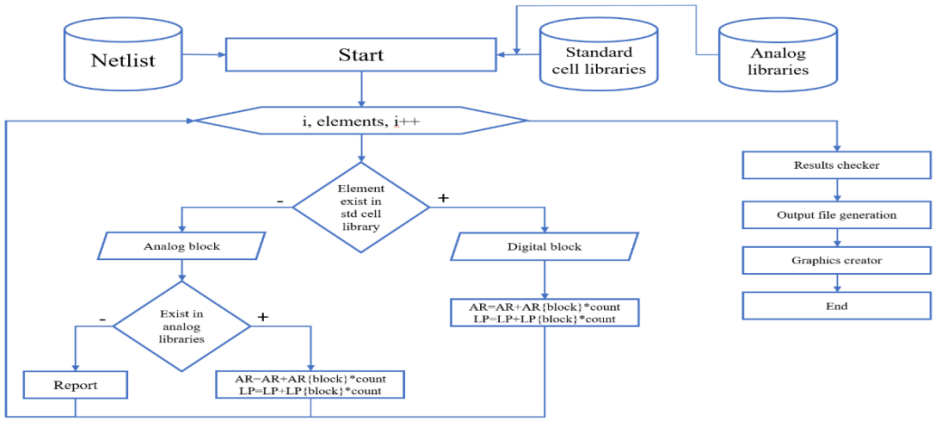

Figure 4. Proposed algorithm

The input for the work of the software is the gate level netlist, analog and standard cell libraries. At the beginning of the work, the elements used are extracted from gate-level netlist and grouping: the number of elements used in the process is determined. Then the presence of the received elements is checked in the library of digital standard elements, in the absence of which it is checked in the library of analog elements, in the absence of the latter it is presented as a missing element. If the corresponding element is found, information from libraries are extracted, which, if multiplied by the amount of application, is added to the result. It should be noted that the measurement is performed at once for all Process-Voltage-Temperature cases, then the results are checked, the results containing the largest number of elements are extracted. Based on the mentioned algorithm, a software tool has been developed, the input information for the software tool is gate-level netlist, digital standard cell library and analog block library. The mentioned libraries can be given for all possible process-voltage-temperatures and the number of mentioned libraries does not affect the speed of the system.

Scientific novelty. CMOS technologies are constantly changing. The increase of the number of transistors in integrated circuits and the reduction in area size is characterized by Gordon Moore's 1965 law, which states that the number of transistors in integrated circuits doubles every one and a half years, now exceeding ten billion. As a result of transistor size scaling - also changing requirements for other parameters in integrated circuits, such as power consumption of integrated circuits. It should be noted that over time, the power consumption requirements of integrated circuits are increasing, as most integrated circuits currently operate in systems for which portable lithium-batteries are the main source of supply. The three main challenges arising from Gordon Moore's law are high speed, small area, and low power consumption. The parameters of the integrated circuits are inversely proportional; the improvement of one lead to deterioration of the other. For example, in multi-core processors, the power consumption is improved

due to the reduction in speed. The total power consumption of integrated cir-cuits consists of two components: dynamic and static (Fig. 1) [Melikyan et al., 2018, 1-5].

Analysis. Mixed-signal integrated circuits were acclimated to test the system, the first being a logic-arithmetic unit and the second a processor belonging to the MSP430 family. For expeditious application of the system, has been developed a graphical inter-face, through which the system input data is provided. Below is the graphical interface.

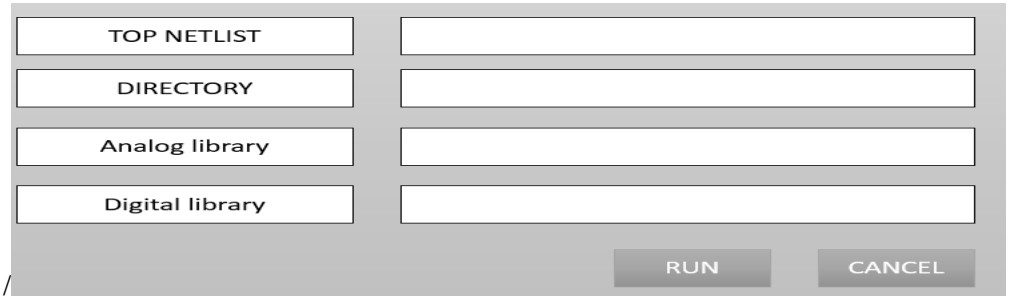

Figure 5. Graphical interface

The directory is optional input, it's connected with the gate-level netlist because in netlist we can have a hierarchical structure where submodules can be in other directory. From the results presented in Table 1 can be concluded that algorithm is 45% or more expeditious, and the precision of the obtained results is deviated by a maximum of 16%.

	Runtime			**Leakage power**		
Elements count	**Classic method**	**Proposed System (s)**	**Difference (%)**	**Classic method**	**Proposed System**	**Difference (%)**
46	32	15	53	3,362	3,762	12
1532	34	19	45	4,5	5,22	16

Table 1. Test results

To make the results more perceptible, in integration to the final text file, graphs are engendered, which are shown in Figure 5, respectively.

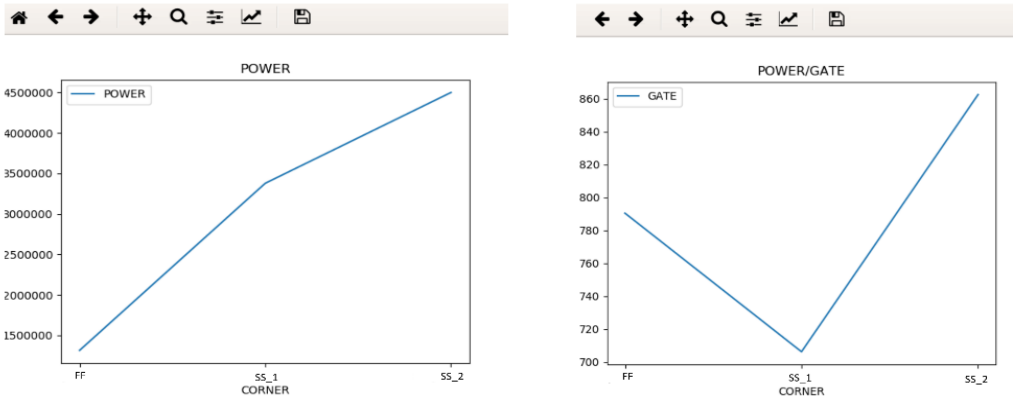

Figure 5. Graphics result

In output text file the result given in corner by corner format. The results show that the presented system will be in demand both for starters and integrators, who mainly have a research function and for astronomically immense organizations that carry out consummate projects. One of the advantages of the system is that it is independent.

Conclusion. During the work, the difficulties of making quantifications in sizably voluminous integrated circuits were studied, which in turn affects the period of market ingression. The optically canvassed complications are mainly connected with the fact that in modern integrated circuits there are analog and digital subunits. An automated system for quantifying the parameters of integrated circuits is introduced, which can be utilized in all stages of integrated circuit design. The presented software it is at least 45% more expeditious than the subsisting approaches, and the quantification error in the results is a maximum of 16%. Utilizing the presented algorithm, information on the parameters of integrated circuits for different process-voltage-temperature processes can be obtained at different stages of design. In additament to tabular version of receiving data, the system exports a graphical interface that is more convenient for visual inspections.

References

1. V. Melikyan, M. Martirosyan, D. Babayan, V. Janpoladov, D. Musayelyan. Multi-Voltage and Multi-Threshold Low Power Design Techniques for ORCA Processor Based on 14 nm technology - 2018 IEEE 38th International Conference on Electronics and Nanotechnology
2. A. Agarwal, S. Mukhopadhyay, A. Raychowdhury, Roy K. Leakage power analysis and reduction for nanoscale circuits- IEeE Micro 2006 26(2) page 692-696
3. Vashishtha V., Gujja A. and Clark L.T. Delay and power tradeoffs for static and dynamic register files // Circuits and Systems (ISCAS): IEEE Int. Symopsium-2015, May page 2900-2903
4. Chowxajyan, H. Verilog-i kirar'owmy' t'vayin hamakargeri naxagc'man gorc'y'nt'acowm - Er&an: E'dit' Print, 2011. - 227 e'j
5. B. Dilip, P. Prasad, R. Bhavani. Leakage Power Reduction In Cmos Circuits Using Leakage Control Transistor Technique In Nanoscale Technology, IJESS, Vol-2 Iss-1, 2012

Davit BABAYAN, Artur GHAZARYAN, Gurgen GRIGORYAN, Tigran GRIGORYAN
Problems of economic and technical and efficiency of integrated circuit parameters
Keyword: digital blocks, analog blocks, leakage power, corner, area, measurement system.

One of the main requirements during the process of designing integrated circuits is TTA (time to market) which is basically the period of the time spend on developing IC chips as well as decreasing power consumption and area. At present, the technology has reached up to 3 nm and most of the designed circuits are used in systems for which the power supply is lithium-based batteries. From what has been said, energy consumption is becoming a more powerful challenge now. Studies have shown that alongside with technology downscaling static energy consumption can be several times greater than dynamic energy consumption. In large integrated circuits, different methods are used to calculate energy consumption, which differ in speed and accuracy. For example, in spice modeling, the exact power consumption of the circuit can be obtained, but in the case of large projects, this can take a very long time. At the same time correctly measuring area or power consumption during development of IC design become a critical point to solve.