ECONOMIC EFFICIENCY OF ASIC PROCESSOR WITH LOW POWER CONSUMPTION DUE TO FFT CALCULATIONS

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Introduction. This paper describes a processor architecture optimized for radix-4 and coupled-radix FFT algorithms, which are simpler than radix-2 algorithms. The processor is based on a transport architecture and several optimizations have been used to improve power efficiency. The processor was synthesized using standard 4nm cell technology, and analysis shows that the programmable solution can achieve energy efficiency comparable to fixed-function ASICs.

FFT has typically been implemented as a fixed function in integrated circuits because it provides better power consumption and performance than software implementations. Such implementations have recently been presented, e.g., in [Wey, 2007,783], implementations based on radix-2 FFTs are presented, and examples of radix-4 FFTs can be found, e.g., in [Hung, 2004, 833-836]. Implementations based on paired-radix algorithms are presented in [Liu, 2007, 44-47].

This article describes a processor architecture optimized for FFT calculations. Several optimizations have been used to improve CPU power consumption. This paper shows that a programmable solution can have an energy consumption comparable to a fixed function. The processor is optimized for radix-4 and conjugate-radix FFT algorithms and supports multiple transform lengths.

FFT Algorithm: The Fast Fourier Transform (FFT) is an algorithm that computes the Discrete Fourier Transform (DFT) of a sequence. FFT can also be used in different ways. Fourier analysis transforms a signal from its original region (often temporal or spatial) to a representation in the frequency domain and vice versa. The DFT is obtained by dividing the sequence of values into components of different frequencies. This operation is useful in many areas, but computing it directly from the definition is often too slow to be practical. FFT quickly computes such transformations by multiplying the FFT matrix by

products of sparse (mostly zero) factors. The speed difference can be huge, especially for long data sets where the order can be in the thousands. In the presence of rounding error, many FFT algorithms are much more accurate. There are many different FFT algorithms based on a wide range of published theories, from simple arithmetic of complex numbers to group theory and number theory.

Methodology. The proposed processor is based on the transport architecture [Corporaal,1997, 330-341], which is a class of statically programmable instruction-level parallelism architectures. In the transport architecture programming model, the program only passes data over the network of interconnections, and the actual operations occur as a "side effect" of the data transfer. The operands of the function block are entered through ports, and one of the ports acts as a trigger. Whenever data is transferred to the trigger port, the function block initiates the action. When the input ports are registered, the operands for the operation can be stored in the registers of previous instruction cycles, and the trigger port transfer starts the operation on the operands stored in the registers. In this way, operands can be distributed between different functions, block operations, reducing data conflicts in the interconnection.

A processor configured for FFT must support a complex data type, and here the data is split into two parts. Complex units of multiplication and addition are also introduced. A complex addition block computes any four-operand operation defined in a 4-point FFT, and the structure is shown in Figure in 1.

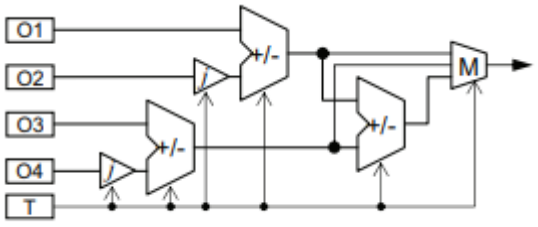

Figure 1. Block diagram of a complex adder

In this block, the opcode is used as a trigger port, so that when four operands are passed to the input ports, the four outputs can be triggered by passing the opcode to the trigger code without having to pass the operands.

Literature review. Currently, when the size of transistors has reached 2 nm [Song, 2019, 1-2], high-speed systems have become more energy-efficient because they have begun to operate at lower supply voltages. The operating frequencies of the systems have reached tens of gigahertz [Patel, 2010, 2-4]. Despite these advantages, it has become

more difficult to ensure stability, reliability and timing constraints in the system. High operating frequencies result in a ASICmatch between clock signals and data signals.

Scientific novelty. Currently, the market for integrated circuits is fixedly growing, and companies whose semiconductor devices do not have flexibility in the face of non-standard conditions are considered uncompetitive. The only way to develop a more competitive product is to develop an integrated circuit that meets the criteria for stability and reliability in an unstable environment. The proposed architecture allows to minimize the power consumption of the processor, which leads to the reduction of the cost and to be more competitive in the market.

Analysis. The processor was designed in Verilog so that the rotation coefficient generator block supports the capacity of two FFT's up to 16 KB, that is, the lookup table of the rotation coefficient block contains 2049 complex coefficients. The device has two pipeline stages and the lookup table is implemented as hard logic. The processor has 32-bit resolution, which allows complex data to be represented using a 16-bit real part and a 16-bit imaginary part. Clock signal protection has been implemented to reduce the power consumption of inactive function blocks. This provides savings on low load units.

The project was synthesized using standard 4 nm cell technology. Energy consumption estimates are obtained using valve-level simulations. Outcome characteristics are shown in Table 1. The rotation factor block uses about 23% of the core area and 7% of the power consumption, so the rotation factor block improves the power efficiency of FFT calculations. The most significant energy savings compared to the previous results of [Pitkanen, 2006, 84-88] are related to the data memory, since two parallel single-port memories were used here instead of two ports, which halved the memory energy consumption.

```
main () {
    initialization (); /* 8 to 42 instructions */
    prologue (); /* 14 instr. */
    for (idx=0; idx <(N⌈log4N⌉)/16-1; idx++)
    kernel (); /* 16 instr. */
    epilogue; /* 17 instr. */
    }
```

Figure 2. Code depicting the structure and management procedure of the program code

The energy efficiency of a FFT implementation is often compared by measuring how many 1024-point FFTs can be calculated with 1 mJ of energy, so a few examples from the literature representing FFTs with different technologies have been selected. The results of the comparison are shown in Table 5.6. The Intel Pentium-4 [Deleganes, 2002, 230-233] is a general-purpose RISC, and the StrongArm SA-1100 [Intel, 1999, 12-16]

can be considered a general-purpose processor for mobile devices because it uses specialized circuit, clock signal protection and supply voltage reduction. Examples of general-purpose DSP processors are the TI TMS320C6416, which is a VLIW machine, and the Imagine [Rixner, 1998,3-13], which is designed for multimedia applications. Both processors use pseudo-ordered data path partitioning. Additionally, the C6416 uses pass-gate multiplexer circuitry. The implementation of FFT on C6416 is described in [Texas Instruments, 2003,11-17]. It should be noted that the 6002 cycle count is achieved through eight memory ports, while the Proposed processor uses only two. The Spiffee processor [18] is designed for FFT, and power consumption is reduced by low supply voltage. An FPGA solution with specially built-in FPGA logic is described in [Lim, 2004, 230-233]. [Wey, 2007, 783-787] report a custom scalable IP core using a single-clock signal-protected memory architecture, and [Wang, 2005, 310-31 9] describe a custom variable-length FFT processor using unidirectional radix-2/4 /8 delay algorithm. A highly optimized FFT implementation using the subthreshold circuit technique is described in [Wang, 2005, 310-319]. A comparison in Table 2 shows that the energy efficiency of the Proposed CPU is equivalent to fixed-function ASIC implementations, even though the implementation is programmable.

Table 1. Specifications of proposed processor synthesized using 4nm ASIC technology

Recommended sizes of FFTs	**64 – 16384**
Number of cycles	207 – 114722
Execution time	828 nm - 459 μs
Energy consumption	60 – 73 mW
Maximum frequency of the clock signal	255 MHz

Table 2. Processor specs by footprint

Nucleus	**38 (*1000 gates)**
Instruction memory	2 (*1000 gates)
Data memory	240 (*1000 gates)
General	280 (*1000 gates)

Table 3. 1024- point FFT

Number of cycles	**5160**
Energy consumption	60.4mW, 0.9V, 250MHz 29.8mW, 0.675V, 140MHz

Table 4. 8192-point FFT

Number of cycles	**5 7396**
Energy consumption	68.7 mW, 0.9 V, 250 MHz

Table 5 . Power consumption comparison for a 1024-point FFT

Project	Technology nm	Power supply V:	t_{clk} : MHz	t_{FFT} mkv	FFT/mJ
Recommended	4	0.9	250	21	809
[Lim, 2004]	4	0.75	100	13	149
[Wey, 2007]	4	0.8	500	8	100
[Deleganes, 2002]	4	0.75	300	24	1
[Rixner, 1998]	7	1.2	232	160	16
[Lim, 2004]	14	1.5	6	430	1428
[Wey, 2007]	14	1.5	20	282	43
[Wang, 2005]	28	1.8	45	23	93

Table 6 . Power consumption comparison for an 8192-point FFT

Recommended	**4**	**0.9**	**250**	**230**	**63**
[Lin, 2004]	14	1,2	20	717	55
[Wey, 2007]	14	1.5	22	908	35
[Liu, 2007]	28	1.8	12	1198	4

Conclusion. This paper proposed a low-power, dedicated processor for FFT calculations that used several techniques to reduce power consumption: special function blocks, parallel memory, clock signal protection, and code compression. The processor was synthesized using 4nm ASIC technology and the power consumption analysis showed that the proposed processor is 26.8% energy efficient without significant performance degradation, which promotes sales volumes by 23%.Performance can even be improved by adding more computing resources.

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Economic Efficiency of a specialized processor with low power consumption due to FFT calculations
Key words: discrete fourier transforms, fast fourier transforms, application specific integrated circuits, digital signal processors, parallel architectures, transport architectures, power consumption, sales promotion

Nowadays when semiconductor device sizes reached a few nanometers, high-speed processors became less power-consuming, and systems operating frequencies reached dozens of gigahertz. Despite these advantages, devices became more vulnerable against temperature-voltage drifts. Also, because of dozens of gigahertz frequency data transASICsion, it became more complicated to meet timing constraints in processors. With the help of FFT calculations, it becomes possible to design more affordable ASIC processors with low power consumption. Currently, the integrated circuit market is fixedly growing, and companies whose semiconductor devices do not have flexibility in non-standard conditions are considered uncompetitive. The only way to develop a more competitive product is to develop an integrated circuit that meets the standards of stability and reliability in unstable conditions. The proposed architecture reduces processor power consumption by 26.8%, which leads to a 23% reduction in costs and increased competitiveness in the market.